Verilog code

module top\_module(

input wire [3:0] sw,

output wire [6:0] a\_to\_g,

output wire [7:0] an,

output wire dp

);

assign an = 8'b11111110;

assign dp = 1;

hex7seg D1(.x(sw), .a\_to\_g(a\_to\_g));

endmodule

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module hex7seg(

input wire [3:0]x,

output reg [6:0]a\_to\_g

);

always@(\*)

begin

case(x)

0: a\_to\_g = 7'b0000001;

1: a\_to\_g = 7'b1001111;

2: a\_to\_g = 7'b0010010;

3: a\_to\_g = 7'b0000110;

4: a\_to\_g = 7'b1001100;

5: a\_to\_g = 7'b0100100;

6: a\_to\_g = 7'b0100000;

7: a\_to\_g = 7'b0001111;

8: a\_to\_g = 7'b0000000;

9: a\_to\_g = 7'b0000100;

'hA: a\_to\_g= 7'b0001000;

'hB: a\_to\_g= 7'b1100000;

'hC: a\_to\_g= 7'b0110001;

'hD: a\_to\_g= 7'b1000010;

'hE: a\_to\_g= 7'b0110000;

'hF: a\_to\_g= 7'b0111000;

default: a\_to\_g = 7'b0000001;

endcase

end

endmodule